

# BGT24MTR11

Silicon Germanium 24 GHz Transceiver MMIC

## Data Sheet

Revision 3.1, 2014-03-25

RF & Protection Devices

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**BGT24MTR11 Silicon Germanium 24 GHz Transceiver MMIC**

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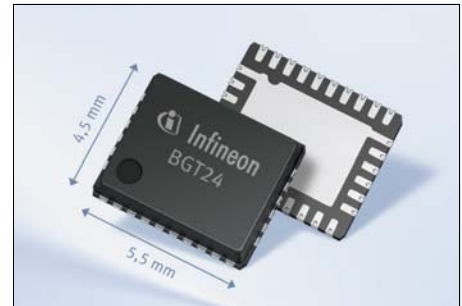
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## 1 Features

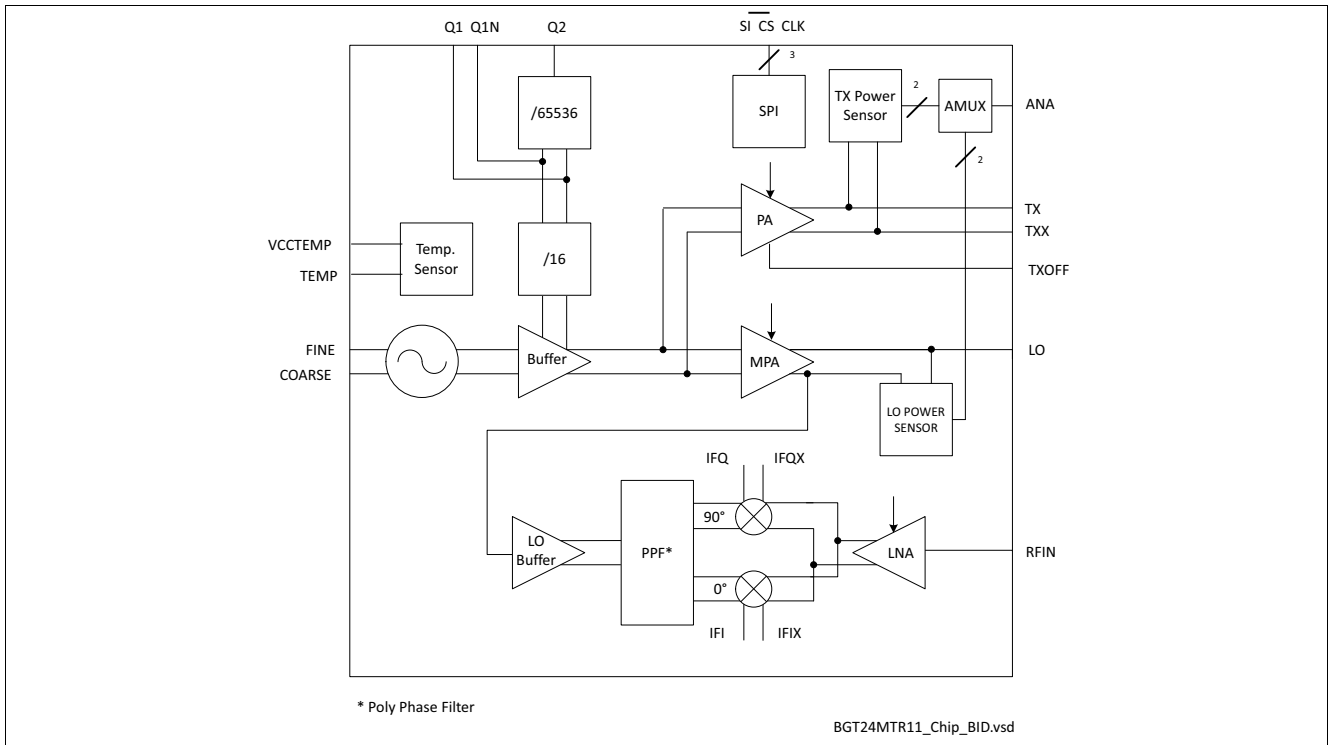
- 24 GHz transceiver MMIC
- Fully integrated low phase noise VCO
- Switchable prescaler with 1.5 GHz and 23 kHz output
- On chip power and temperature sensors
- Gilbert based homodyne quadrature receiver
- Single ended RF and LO terminals
- Low noise figure  $NF_{SSB}$ : 12 dB
- High conversion gain: 26 dB
- High 1 dB input compression point: -12 dBm
- Single supply voltage 3.3 V
- Power consumption 500 mW in continuous operating mode
- 200 GHz bipolar SiGe:C technology b7hf200
- Fully ESD protected device
- VQFN-32-9 leadless plastic package incl. LTI feature
- Pb-free (RoHS compliant) package



### Description

The BGT24MTR11 is a Silicon Germanium MMIC for signal generation and reception, operating from 24.0 up to 26.0 GHz. It is based on a 24 GHz fundamental voltage controlled oscillator. Switchable frequency prescalers are included with output frequencies of 1.5 GHz and 23 kHz. The main RF output delivers typ. 11dBm signal power to feed an antenna and an auxiliary LO output is available to provide LO signal to separate receiver components. A LNA provides low noise figure and a RC polyphase filter (PPF) is used for LO quadrature phase generation of the homodyne quadrature downconversion mixer. Output power sensors as well as a temperature sensor are implemented for monitoring purposes. The device is controlled via SPI and is manufactured in a 0.18 $\mu$ m SiGe:C technology offering a cutoff frequency of 200 GHz. The MMIC is packaged in a 32 pin leadless RoHS compliant VQFN package.

Product Name	Package	Chip	Marking
BGT24MTR11	VQFN32-9	T1524	BGT24MTR11



**Figure 1 BGT24MTR11 Block Diagram**



## 2 Electrical Characteristics

### 2.1 Absolute Maximum Ratings

$T_A = -40\text{ °C}$  to  $105\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)<sup>1)</sup>

**Table 1 Absolute Maximum Ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC} / V_{CCTEMP}$	-0.3	–	3.6	V	–
DC voltage at RF Pins TX, TXX, LO, RFIN1, RFIN2	$VDC_{RF}$	0	–	0	V	MMIC provides short circuit to GND for all RF pins
DC voltage at Pins IFI, IFIX, IFQ, IFQX	$VDC_{IF}$	0	–	Vcc	V	–
DC current into Pins IFI, IFIX, IFQ, IFQX	$I_{IF}$	-8.5	–	3.5	mA	Max. values indicate current due to short circuit to GND and Vcc resp.
DC voltage at Pin ANA	$VDC_{ANA}$	-0.3	–	3.6	V	–
DC current into Pin ANA (Sink)	$I_{ANA\ SINK}$	125	350	500	$\mu$ A	Max. values indicate current due to short circuit to GND and Vcc resp.
DC current into Pin ANA (Source)	$I_{ANA\ SOURCE}$	-7	–	–	mA	–
DC current into Pin VCCTEMP	$I_{VCCTEMP}$	–	–	3.5	mA	Max. values indicate current due to short circuit to GND and Vcc resp.
DC voltage at Pin TEMP	$VDC_{TEMP}$	0	–	Vcc	V	–
DC current into Pin TEMP	$I_{TEMP}$	-1	–	1.5	mA	Max. values indicate current due to short circuit to GND and Vcc resp.
DC voltage at Pins Q1, Q1N	$VDC_{Q1x}$	Vcc-0.3	–	Vcc	V	–
DC current into Pins Q1, Q1N	$I_{Q1x}$	-8	–	12	mA	–
DC voltage at Pin Q2	$VDC_{Q2}$	-0.3	–	3.6	V	–
DC current into Pin Q2 enabled	$I_{Q2EN}$	-3	–	3	mA	–
DC current into Pin Q2 disabled	$I_{Q2DIS}$	-10	–	10	$\mu$ A	–
DC voltage at SPI input Pins SI, CLK, $\overline{CS}$	$VDC_{SPIIN}$	-0.3	–	3.6	V	–
DC current into SPI input Pins SI, CLK, $\overline{CS}$	$I_{SPIIN}$	–	–	3	mA	–
RF input power into Pin RFIN	$P_{RF}$	–	–	0	dBm	–

1) Not subject to production test, specified by design

**Table 1 Absolute Maximum Ratings (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC voltage at Pins Fine, Coarse	$V_{\text{Fine}}, V_{\text{Coarse}}$	0	–	5	V	–
DC current into Pins Fine, Coarse	$I_{\text{Fine}}, I_{\text{Coarse}}$	-1	–	0.11	mA	Positive currents if $V_{\text{TUNE}} > V_{\text{CC}}$
DC voltage at Pin TXOFF	$VDC_{\text{TXOFF}}$	-0.3	–	3.6	V	–
Total power dissipation	$P_{\text{DISS}}$	–	–	750	mW	With BIST deactivated
Junction temperature	$T_{\text{J}}$	-40	–	150	°C	–
Ambient temperature range	$T_{\text{A}}$	-40	–	105	°C	$T_{\text{A}}$ = temperature at package soldering point
Storage temperature range	$T_{\text{STG}}$	-40	–	150	°C	–

**Attention: Stresses exceeding the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

## 2.2 Thermal Resistance

**Table 2 Thermal Resistance**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction - soldering point <sup>1)</sup>	$R_{\text{thJS}}$	–	–	40	K/W	–

1) For calculation of  $R_{\text{thJA}}$  please refer to application note thermal resistance

## 2.3 ESD Integrity

**Table 3 ESD Integrity**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD robustness, HBM <sup>1)</sup>	$V_{\text{ESD-HBM}}$	-1	–	1	kV	All pins
ESD robustness, CDM <sup>2)</sup>	$V_{\text{ESD-CDM}}$	-500	–	500	V	All pins

- 1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kΩ, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level
- 2) According to JEDEC JESD22-C101 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

## 2.4 Measured RF Characteristics

### 2.4.1 Power Supply

**Table 4** Typical Characteristics  $T_A = -40 \dots 105 \text{ }^\circ\text{C}$ , SPI-Bit 4 = high

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	3.135	3.3	3.465	V	–
Supply current	$I_{CC}$	110	150	190	mA	Supply current typ. 5mA decreased if SPI-Bit 4 = low
Supply voltage temperature sensor	$V_{CCTemp}$	3.135	3.3	3.465	V	–
Supply current temperature sensor	$I_{CCTemp}$	1.3	2.2	3	mA	–

### 2.4.2 TX Section

**Table 5** Typical Characteristics  $T_A = -40 \dots 105 \text{ }^\circ\text{C}$  for  $f = 24.0 \dots 25.5 \text{ GHz}$  or  $T_A = -40 \dots 85 \text{ }^\circ\text{C}$  for  $f = 24.0 \dots 26.0 \text{ GHz}$ , SPI-Bit 4 = high<sup>1)</sup>

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO frequency range	$f_{VCO}$	24.0	–	26.0	GHz	@ $T_A \leq 85^\circ\text{C}$ and $V_F = V_C$
VCO frequency range	$f_{VCO}$	24.0	–	25.5	GHz	@ $T_A \leq 105^\circ\text{C}$ and $V_F = V_C$
VCO fine tuning voltage <sup>2)</sup>	$V_F$	0.5 <sup>3)</sup>	–	5 <sup>4)</sup>	V	–
VCO coarse tuning voltage <sup>2)</sup>	$V_C$	0.5 <sup>3)</sup>	–	5 <sup>4)</sup>	V	–
VCO tuning slope FINE	$\Delta f / \Delta V_F$	–	–	1500	MHz/V	–
VCO tuning slope COARSE	$\Delta f / \Delta V_C$	–	–	3000	MHz/V	–
VCO temperature drift	$\Delta f / \Delta T$	-10	-6	0	MHz/K	Min. @ $T = -40^\circ\text{C}$
VCO pushing	$\Delta f / \Delta V_{CC}$	-350	60	350	MHz/V	Absolute values
VCO phase noise	$P_N$	–	-85	-75	dBc/Hz	@ 100kHz offset, $V_F = V_C$
TX/TXX load impedance	$Z_{TX}$ $Z_{TXX}$	–	19.8-j20.9 18-j17.3	–	$\Omega$	Typical value at 24.125GHz and $VSWR \leq 2:1$
Max. TX output power	$P_{TX}$	5	11	15	dBm	$24.0\text{GHz} \leq f \leq 26.0\text{GHz}$
Max. TX output power for ISM band	$P_{TXISM}$	6	11	15	dBm	$24.0\text{GHz} \leq f \leq 24.25\text{GHz}$

**Table 5** Typical Characteristics  $T_A = -40 \dots 105 \text{ }^\circ\text{C}$  for  $f = 24.0 \dots 25.5 \text{ GHz}$  or  $T_A = -40 \dots 85 \text{ }^\circ\text{C}$  for  $f = 24.0 \dots 26.0 \text{ GHz}$ , SPI-Bit 4 = high<sup>1)</sup> (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TX output power adjustable range	$a_{TX}$	3	9	–	dB	Adjustable via SPI
TX output power in “off” mode <sup>5)</sup>	$P_{TXoff}$	–	–	-30	dBm	Parameter based on IFX eval board design
LO load impedance	$Z_{LO}$	–	24.4-j25.8	–	$\Omega$	Typical value at 24.125GHz and VSWR $\leq$ 2:1
LO output power <sup>6)</sup>	$P_{LO}$	-8	0	6	dBm	SPI-Bit 4 = high
Q1 Prescaler division ratio	$D_{Q1}$	–	2 <sup>4</sup>	–	–	–
Q1 Prescaler output power	$P_{Q1}$	-13	-9	-5	dBm	Q1 loaded with 100 Ohm (AC- coupled)
Q1 load impedance	$Z_{Q1}$	–	100	–	$\Omega$	–
Q2 Prescaler division ratio	$D_{Q2}$	–	2 <sup>20</sup>	–	–	–
Q2 Prescaler max. output voltage	$V_{maxQ2}$	2.4	–	–	V	Test condition: Q2 loaded with high impedance probe (1 MOhm, 13 pF)
Q2 Prescaler min. output voltage	$V_{minQ2}$	–	–	0.8	V	Test condition: Q2 loaded with high impedance probe (1 MOhm, 13 pF)
Q2 Prescaler max. output source current	$I_{maxsource Q2}$	1.2	–	–	mA	Test condition: Q2 loaded with 50 Ohm to Vcc
Q2 Prescaler max. output sink current	$I_{maxsink Q2}$	1.2	–	–	mA	Test condition: Q2 loaded with 50 Ohm to Vcc
Q2 Prescaler output resistance in disable mode	$R_{Q2,DIS}$	100	–	–	k $\Omega$	–
Voltage at Txoff for disabling TX output power	$V_{TX,OFF}$	1.5	–	–	V	–
Voltage at Txoff for enabling TX output power	$V_{TX,ON}$	–	–	0.5	V	–
TXon/off switching time	$t_{ON/OFF}$	–	–	500	ns	–

- 1) Performance based on Application Circuit Figure 2 on Page 15, Cross Section of Application Board, Compensation Structures and Application Board Layout Figure 4 on Page 20ff and Footprint Figure 8 on Page 23
- 2) At tuning pins chipinternal pull-up of 60k $\Omega$   $\pm$  20% to VCC; max.- and min. temperature tuning voltage limits are chosen in a way that they can be linearly interpolated within operating temperature range
- 3) Min. limit @ 25 $^\circ\text{C}$  = 0.8V; min. limit @ 105 $^\circ\text{C}$  = 1.15V
- 4) Max. limit for max. frequency of 24.25GHz = 3.1V; max. limit for max. frequency of 24.5GHz = 3.8V
- 5) Guaranteed by device design
- 6) High LO buffer output power in “high” mode otherwise typ. 4dB reduced LO-output power

### 2.4.3 RX Section

**Table 6** Typical Characteristics  $T_A = -40 \dots 105 \text{ }^\circ\text{C}$  for  $f = 24.0 \dots 25.5 \text{ GHz}$  or  $T_A = -40 \dots 85 \text{ }^\circ\text{C}$  for  $f = 24.0 \dots 26.0 \text{ GHz}$ , SPI-Bit 4 = high<sup>1)</sup>

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO frequency range	$f_{VCO}$	24.0	–	26.0	GHz	@ $T_A \leq 85^\circ\text{C}$
VCO frequency range	$f_{VCO}$	24.0	–	25.5	GHz	@ $T_A \leq 105^\circ\text{C}$
RFIN port impedance <sup>2)</sup>	$Z_{RFIN}$	–	22.9-j14.9	–	$\Omega$	Typical value at 24.125GHz and VSWR $\leq$ 2:1
RFIN VSWR	VSWR	–	–	2:1	–	At source port of off-chip compensation network as proposed
IF frequency range	$f_{IF}$	0	–	10	MHz	–
IF output impedance	$Z_{IF}$	850	1000	1150	$\Omega$	–
Leakage LO to RFIN	$L_{LO \rightarrow RFIN}$	–	–	-30	dBm	Parameter based on IFX eval board design
Voltage conversion gain <sup>3)</sup>	$G_C$	18	26	31	dB	$R_{LOAD,IF} > 10 \text{ k}\Omega$
LNA gain reduction	$\Delta G_{CLG}$	3	5	8	dB	–
SSB noise figure	$N_{SSB}$	–	12	20	dB	Single sideband at $f_{IF} = 100 \text{ kHz}$
IF 1/f corner frequency	$f_c$	–	10	20	kHz	–
Input compression point	$IP_{1dB}$	-17	-12	–	dBm	–
Input 3 <sup>rd</sup> order intercept point	$IIP3$	-8	-4	–	dBm	–
Quadrat. phase imbalance	$\varepsilon_p$	-10	–	10	deg	–
Quadrat. amplitude imbalance	$\varepsilon_A$	-1	–	1	dB	–

1) Performance based on Application Circuit Figure 2 on Page 15, Cross Section of Application Board, Compensation Structures and Application Board Layout Figure 4 on Page 20ff and Footprint Figure 8 on Page 23

2) Guaranteed by device design

3) Lowest gain at high temperature, highest gain at low temperature

## 2.5 Temperature Sensor

Monitoring of the chip temperature is provided by the on-chip temperature sensor which delivers temperature-proportional voltage to the TEMP output. The temp. sensor can be independently biased through VCCTEMP. Thereby the chip temperature can be monitored while the main supply of the transceiver is switched off.

**Table 7 Typical Characteristics Temperature Sensor  $T_A = -40 \dots 105 \text{ }^\circ\text{C}^1$**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature range	$T_{\text{TSENS}}$	-40	–	105	$^\circ\text{C}$	–
Output temperature voltage	$V_{\text{OUT,TEMP}}$	–	1.50	–	V	@ 25 $^\circ\text{C}$
Sensitivity	$S_{\text{TSENS}}$	–	4.5	–	mV/K	–
Overall accuracy error	$Err_{\text{TSENS}}$	–	–	$\pm 15$	K	–

1) all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

## 2.6 Power Detector

For RF output power indication, peak voltage detectors are connected to the output of the TX power amplifier and to the LO medium power amplifier. To eliminate temperature and supply voltage variations, a reference output voltage  $V_{\text{REF}}$  is available through the ANA output for the TX and LO power sensor. The compensated detector output voltage is given by the difference between  $V_{\text{OUT}}$  and  $V_{\text{REF}}$  for both power sensors respectively. This voltage is proportional to the RF voltage swing at the individual amplifier outputs, its characteristic is non-directional.

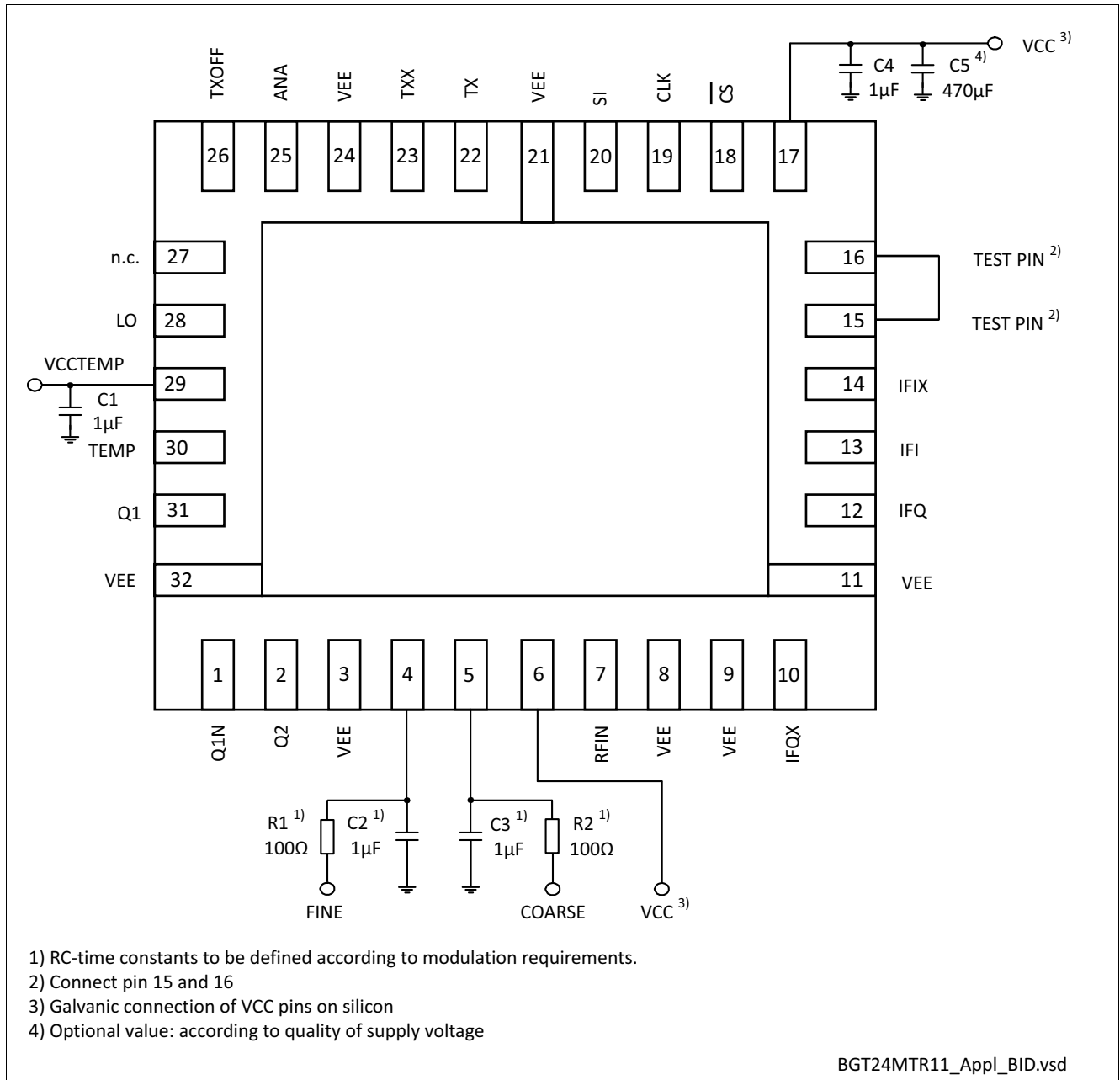
**Table 8 Typical Characteristics Power Detector  $T_A = -40 \dots 105 \text{ }^\circ\text{C}$ ,  $V_{\text{CC}} = 3.3 \text{ V}^1$**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power range	$P_{\text{PSENS}}$	-10	–	15	dBm	–
TX power sensor output	$V_{\text{OUT,TX}} - V_{\text{REF,TX}}$	–	550	–	mV	@ $P_{\text{TX}} = 11 \text{ dBm}$
LO power sensor output	$V_{\text{OUT,LO}} - V_{\text{REF,LO}}$	–	50	–	mV	@ $P_{\text{LO}} = 0 \text{ dBm}$

1) all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

### 3 Application Circuit and Block Diagram

#### 3.1 Application Circuit Schematic



**Figure 2 Application Circuit with Chip Outline (Top View)**

**Table 9 Bill of Materials**

Part Number	Part Type	Manufacturer	Size	Comment
C1 ... C5	Chip capacitor	Various	Various	–
R1 ... R2	Chip resistor	Various	0402	–

### 3.2 Pin Description

**Table 10 Pin Definition and Function**

Pin No.	Name	Function
1	Q1N	Complementary prescaler output 1.5GHz
2	Q2	Prescaler output 23kHz
3	VEE	Ground
4	FINE	VCO fine tuning input
5	COARSE	VCO coarse tuning input
6	VCC	Supply voltage; Total current divided equal on both VCC pins
7	RFIN	RF input downconverter
8	VEE	Ground
9	VEE	Ground
10	IFQX	Complementary quadrature phase IF output downconverter
11	VEE	Ground
12	IFQ	Quadrature phase IF output downconverter
13	IFI	In phase IF output downconverter
14	IFIX	Complementary in phase IF output downconverter
15	TEST PIN	Test pin; DC coupled pin
16	TEST PIN	Test pin; DC coupled pin
17	VCC	Supply voltage; Total current divided equal on both VCC pins
18	$\overline{CS}$	Chip select input SPI (inverted)
19	CLK	Clock input SPI interface
20	SI	Data input SPI interface
21	VEE	Ground
22	TX	Transmit output
23	TXX	Complementary transmit output
24	VEE	Ground
25	ANA	Analog output
26	TXOFF	Pulsable Pin / Please connect to VEE in case TXOFF function is controlled via SPI
27	n.c.	Not connected
28	LO	LO output
29	VCCTEMP	Temperature sensor supply voltage
30	TEMP	Temperature sensor output
31	Q1	Prescaler output 1.5GHz
32	VEE	Ground



### 3.3 SPI

1.) Three signals control the serial peripheral interface of the BGT24MTR11:

SI (Data); CLK (Clock);  $\overline{CS}$  (Chip select)

2.) The data bits SI (MSB first) are read in the shift register with falling edge of the CLK signal.

Please make sure, that the data is present at least 10 ns before and at least 10 ns after the falling edge of the clock signal.

3.) The CLK and  $\overline{CS}$  signals are combined internally.

At least 20 ns before first rising edge of the first CLK signal  $\overline{CS}$  needs to be in "low" state.

While the Data is read,  $\overline{CS}$  has to remain in "low" state.

4.) When Data read in is finished, the shift register content will be written in the latch at the rising edge of the  $\overline{CS}$  signal. The time between the last falling edge of the CLK signal and the rising edge of the  $\overline{CS}$  must be at least 20 ns.

**Table 11 SPI Data Bit Description**

Data Bit	Name	Description (Logic High)	Power ON State
15 (MSB)	GS	LNA Gain reduction	low
14 ..13	–	Not used	low
12	DIS_PA	TX power disabled, in case TXon/off function is controlled via TXOFF pin, this bit needs to be set in low state	high
11	AMUX2	Analog multiplexer control bit 2	high
10	Test Bit	Test bit, must be low otherwise malfunction	low
9	Test Bit	Test bit, must be low otherwise malfunction	low
8	AMUX1	Analog multiplexer control bit 1	low
7	AMUX0	Analog multiplexer control bit 0	low
6	DIS_DIV64k	Disable 64k divider	low
5	DIS_DIV16	Disable 16 divider	low
4	PC2_BUF	High LO buffer output power in "high" mode otherwise typ. 4dB reduced LO-output power	low
3	PC1_BUF	High TX buffer output power	low
2	PC2_PA	TX power reduction bit 2	high
1	PC1_PA	TX power reduction bit 1	high
0	PC0_PA	TX power reduction bit 0	high

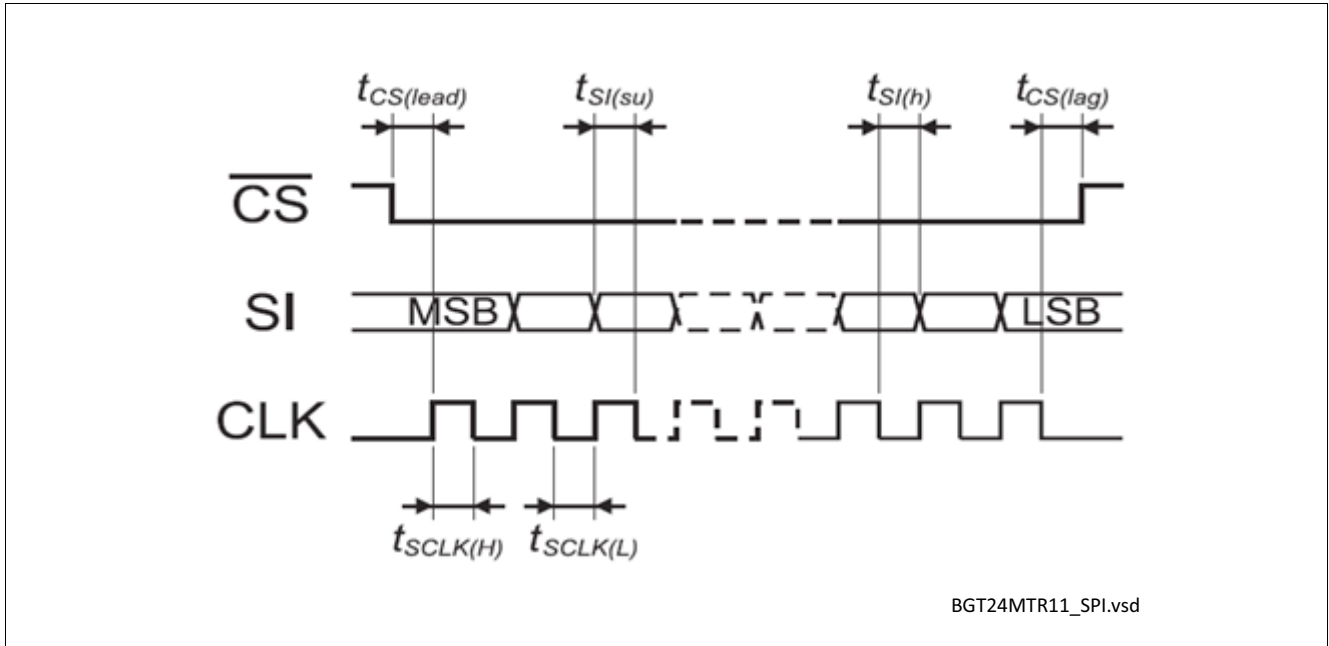


Figure 3 Timing Diagram of the SPI

Table 12 SPI Timing and Logic Levels

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Serial clock frequency	$f_{SCLK}$	0	–	50	MHz
Serial clock high time	$f_{SCLK(H)}$	10	–	–	ns
Serial clock low time	$t_{SCLK(L)}$	10	–	–	ns
Chip select lead time	$t_{CS(lead)}$	20	–	–	ns
Chip select lag time	$t_{CS(lag)}$	20	–	–	ns
Data setup time	$t_{SI(su)}$	10	–	–	ns
Data hold time	$t_{SI(h)}$	10	–	–	ns
Low level (SI, CLK, $\overline{CS}$ )	$V_{IN(L)}$	0	–	0.8	V
High level (SI, CLK, $\overline{CS}$ )	$V_{IN(H)}$	2.0	–	$V_{CC}$	V
Input capacitance (SI, CLK, $\overline{CS}$ )	$C_{IN}$	–	–	2	pF
Input current (SI, CLK, $\overline{CS}$ )	$I_{IN}$	-150	–	150	$\mu A$

Table 13 Truth Table AMUX

Output signal ANA	AMUX2	AMUX1	AMUX0
$V_{OUT,TX}$	low	low	low
$V_{REF,TX}$	low	low	high
$V_{OUT,LO}$	low	high	low
$V_{REF,LO}$	low	high	high
$V_{TEMP}$	high	low	low
Test_Signal1	high	low	high

**Table 13 Truth Table AMUX (cont'd)**

<b>Output signal ANA</b>	<b>AMUX2</b>	<b>AMUX1</b>	<b>AMUX0</b>
Test_Signal2	high	high	low
Test_Signal2	high	high	high

### 3.4 Application Board and Reflow Profile

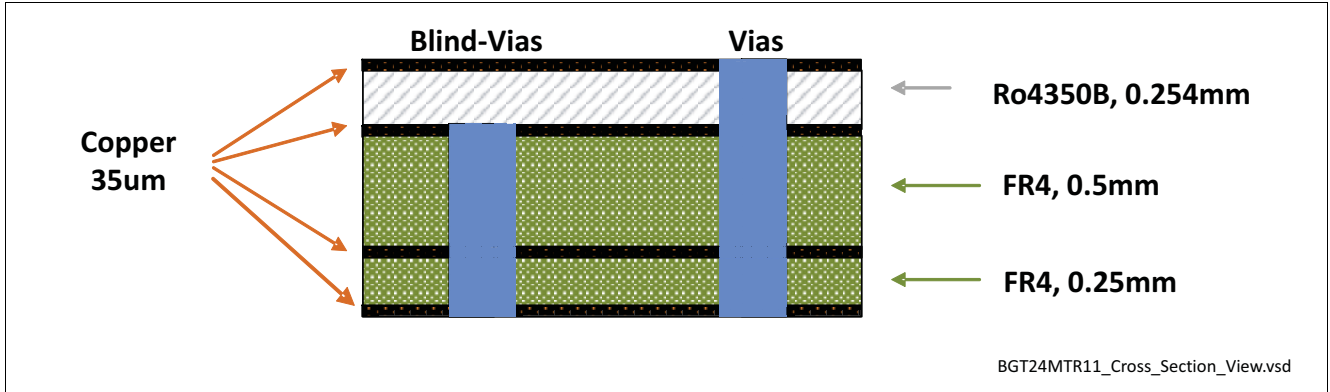


Figure 4 Cross-Section View of Application Board

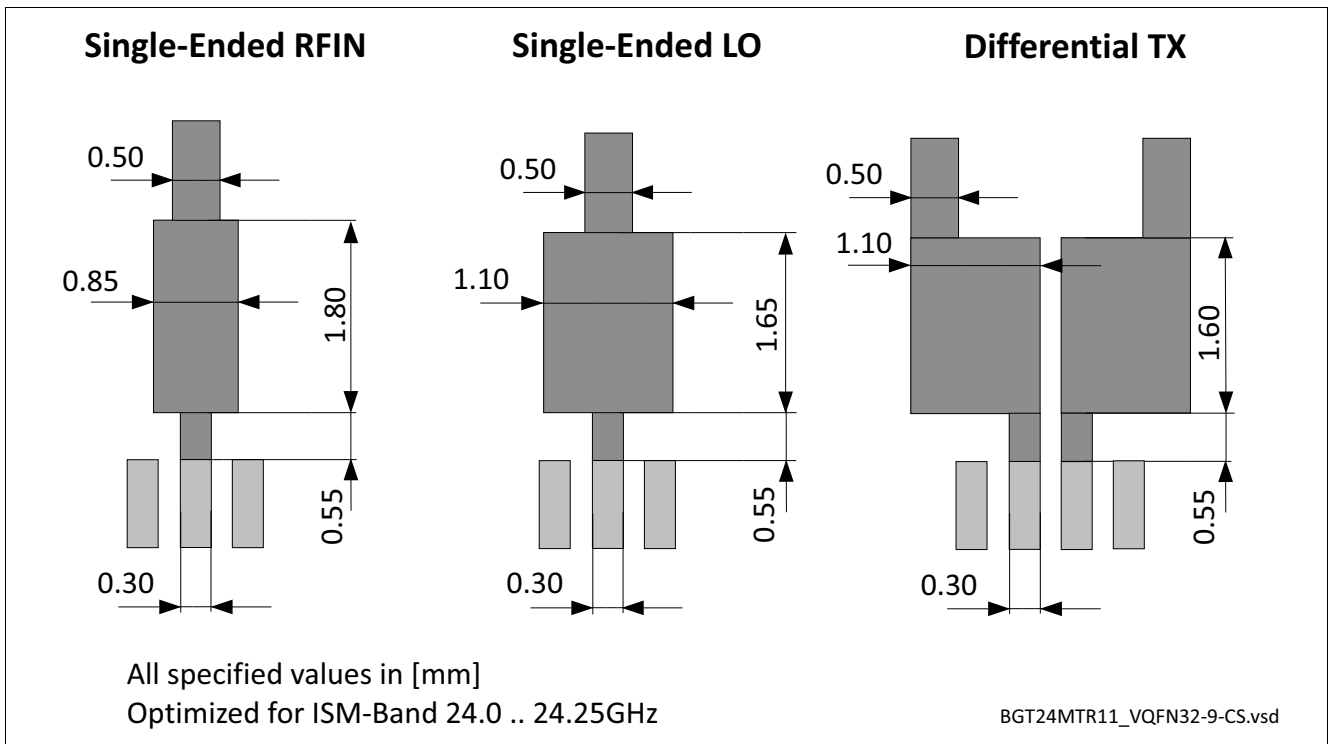
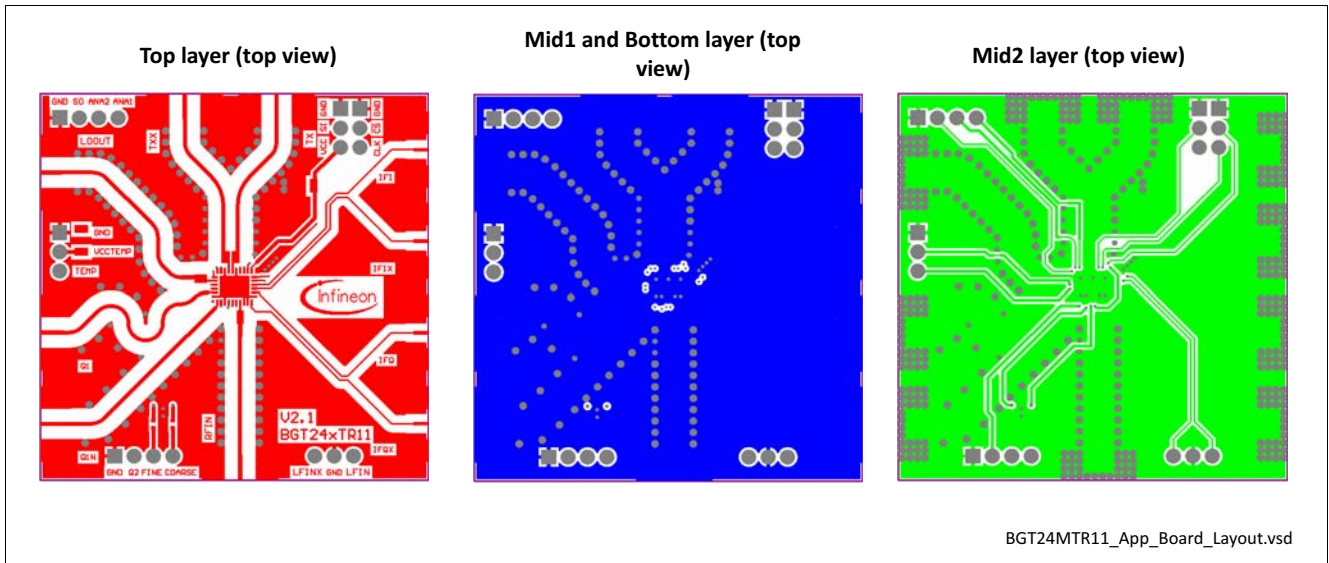


Figure 5 Detail of Compensation Structure (valid for appl. board mat. Ro4350B, 0.254mm acc. to Fig. 5)



**Figure 6 Application Board Layout**

*Note: In order to achieve the same performance as given in this datasheet please follow the suggested PCB-layout. The compensation structure is critical for RF performance. Via holes as recommended on one of next pages (not shown above).*

### 3.5 Equivalent Circuit Diagram of MMIC Interfaces

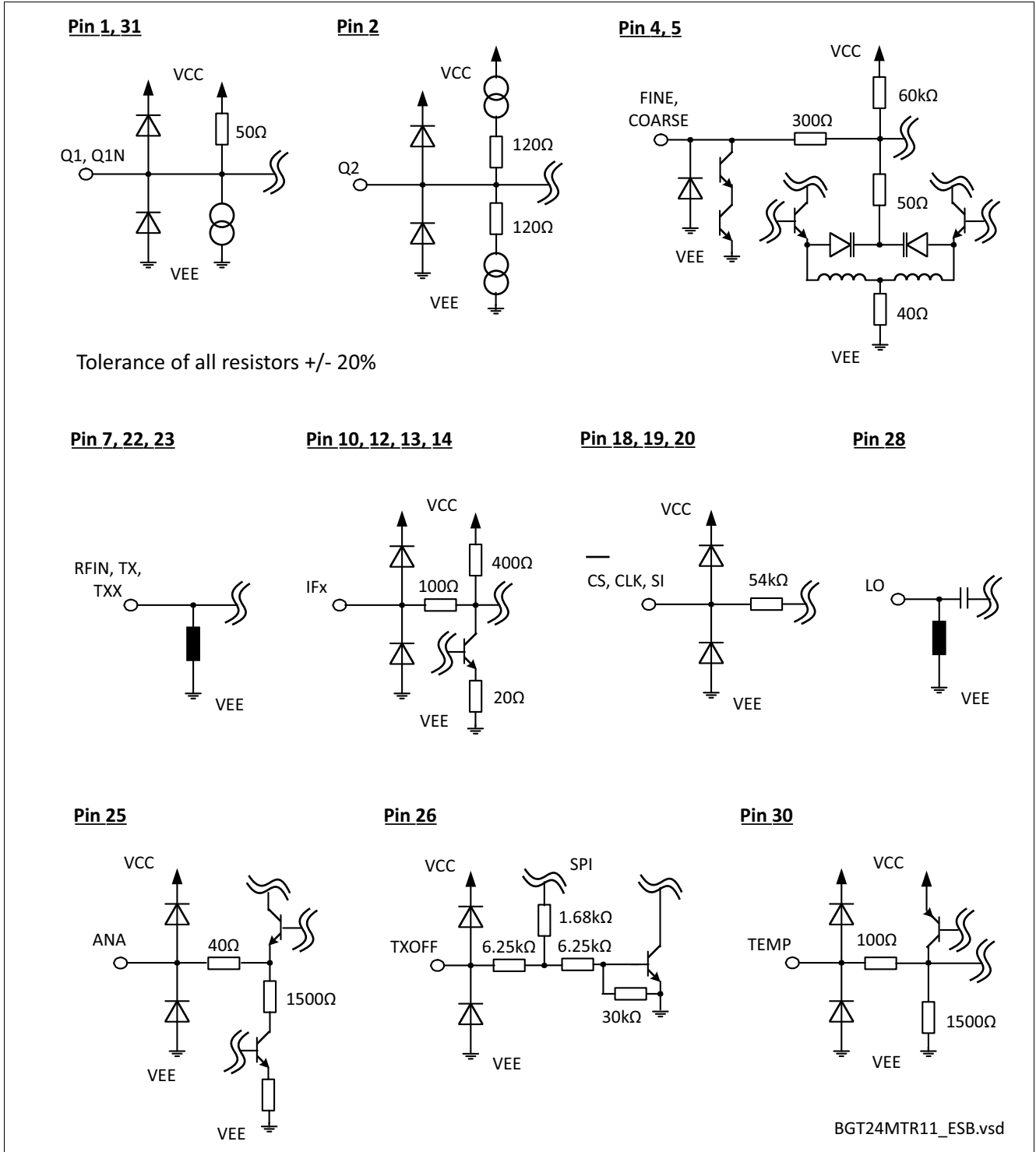


Figure 7 Equivalent Circuit Diagram of MMIC Interfaces

## 4 Physical Characteristics

### 4.1 Package Footprint

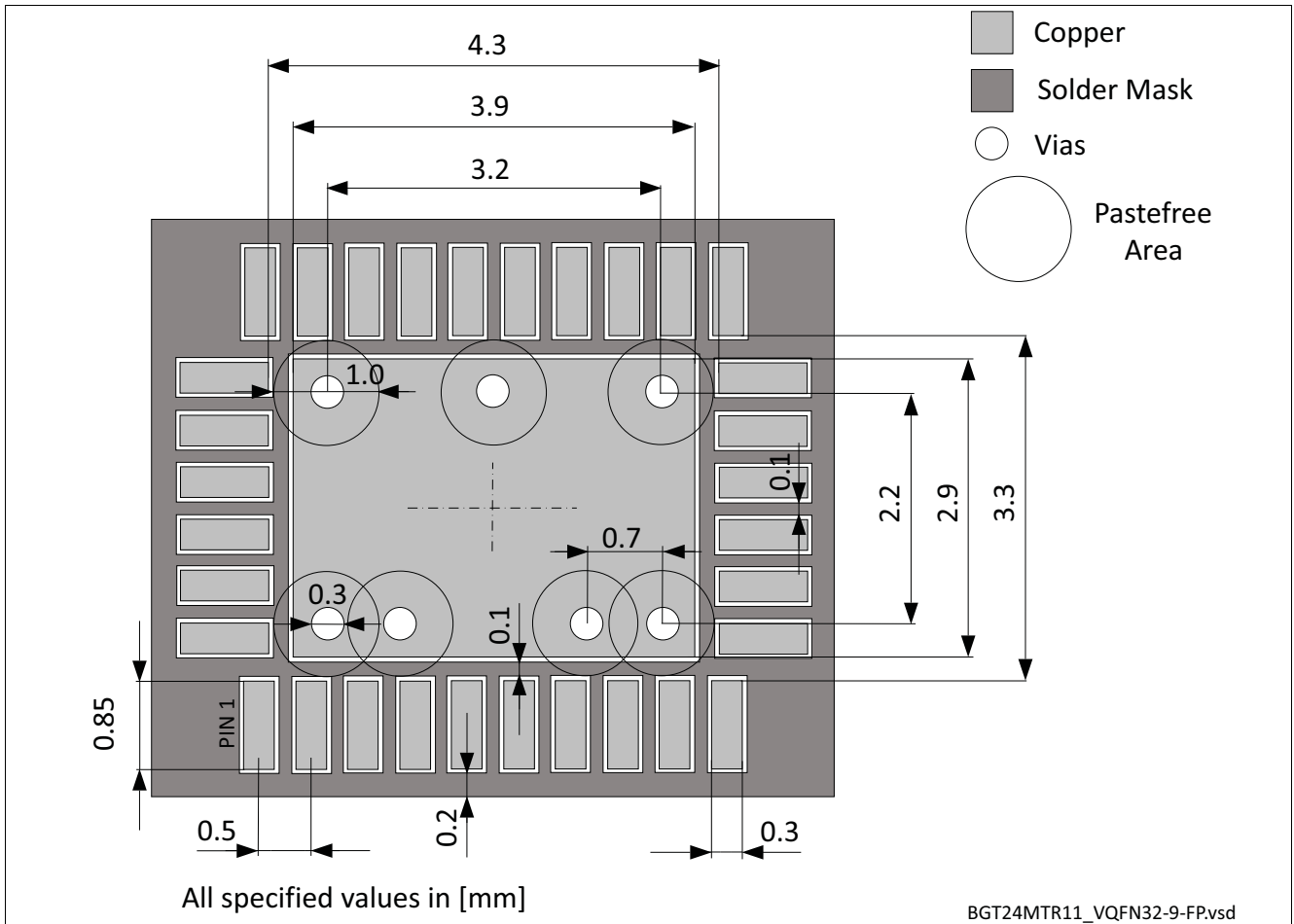


Figure 8 Recommended Footprint and Stencil Layout for the VQFN32-9 Package

## 4.2 Reflow Profile

Soldering process qualified during qualification with "Preconditioning MSL-3: 30°C. 60%r.h., 192h, according to JEDEC JSTD20".

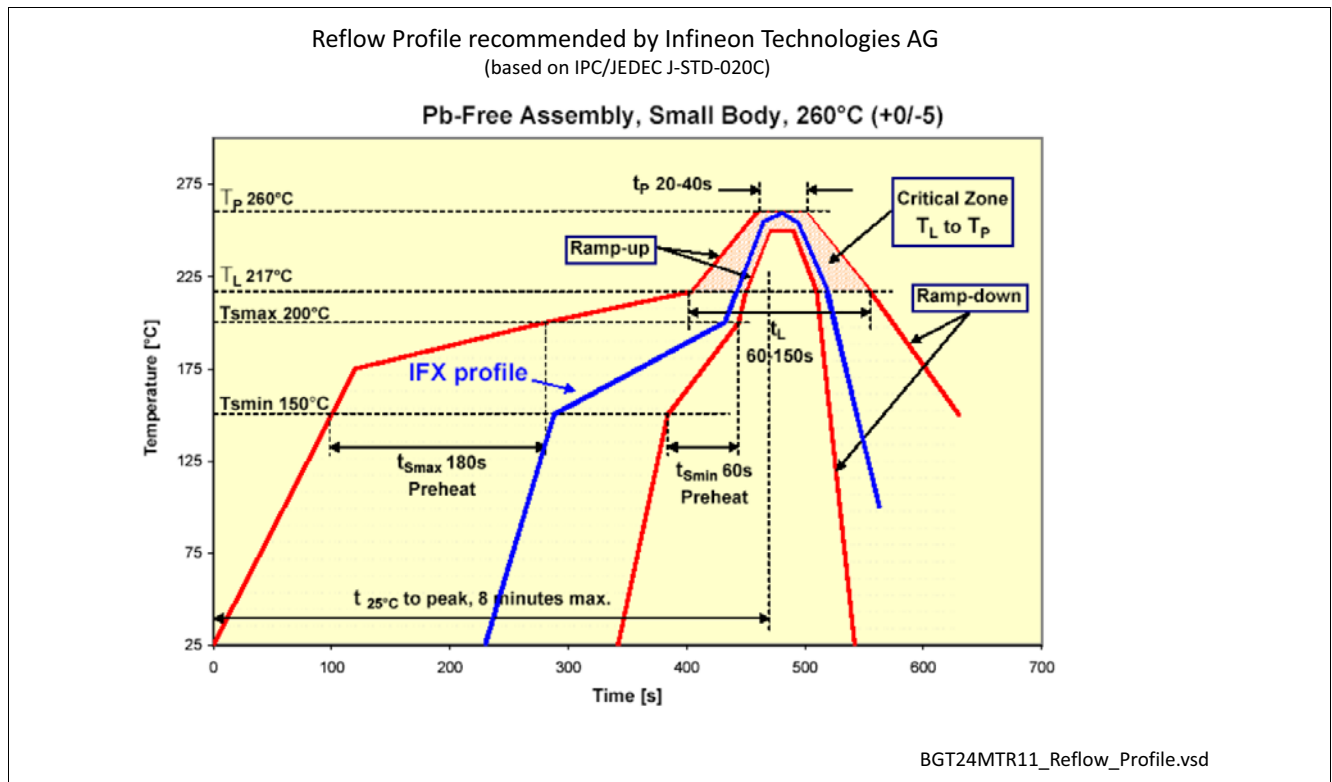


Figure 9 Reflow Profile for BGT24MTR11 (VQFN32-9)



4.3 Package Dimensions

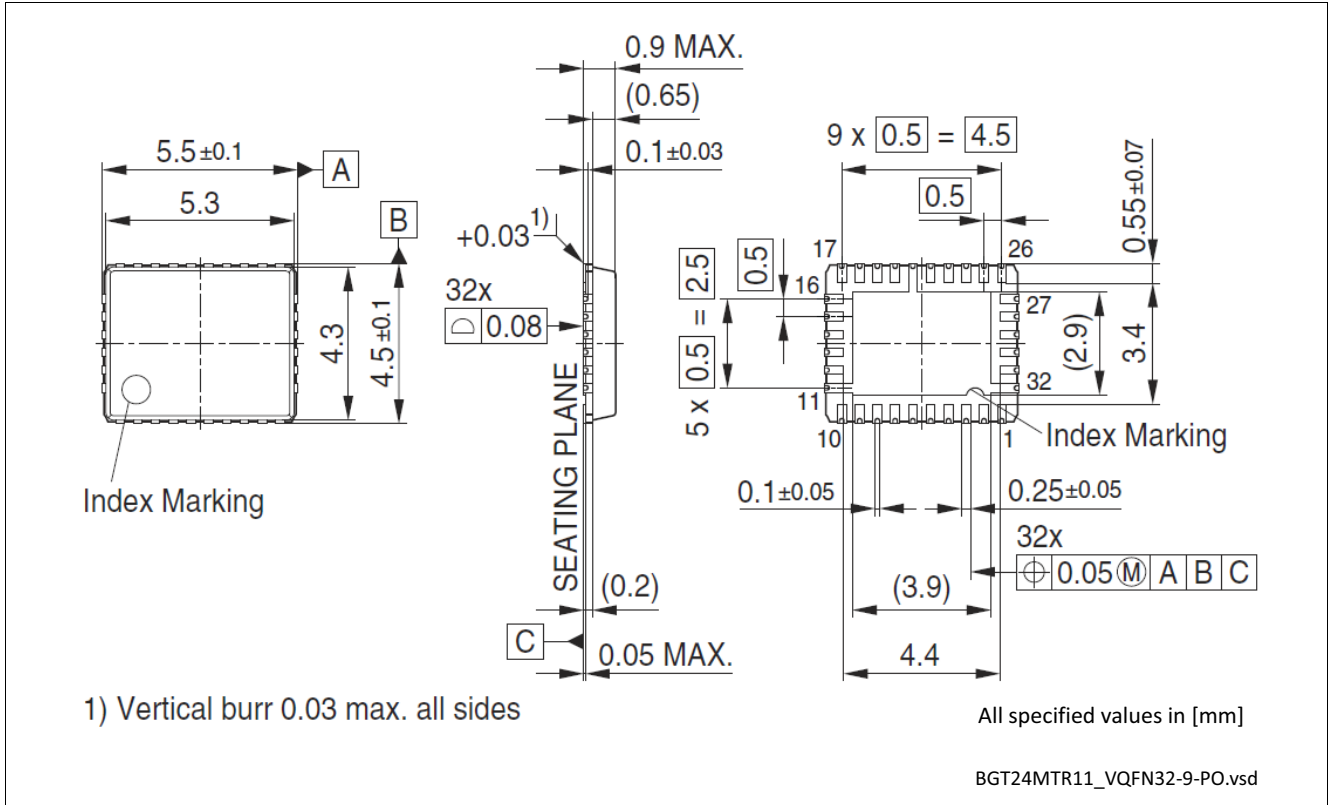


Figure 10 Package Outline (Top, Side and Bottom View) of VQFN32-9

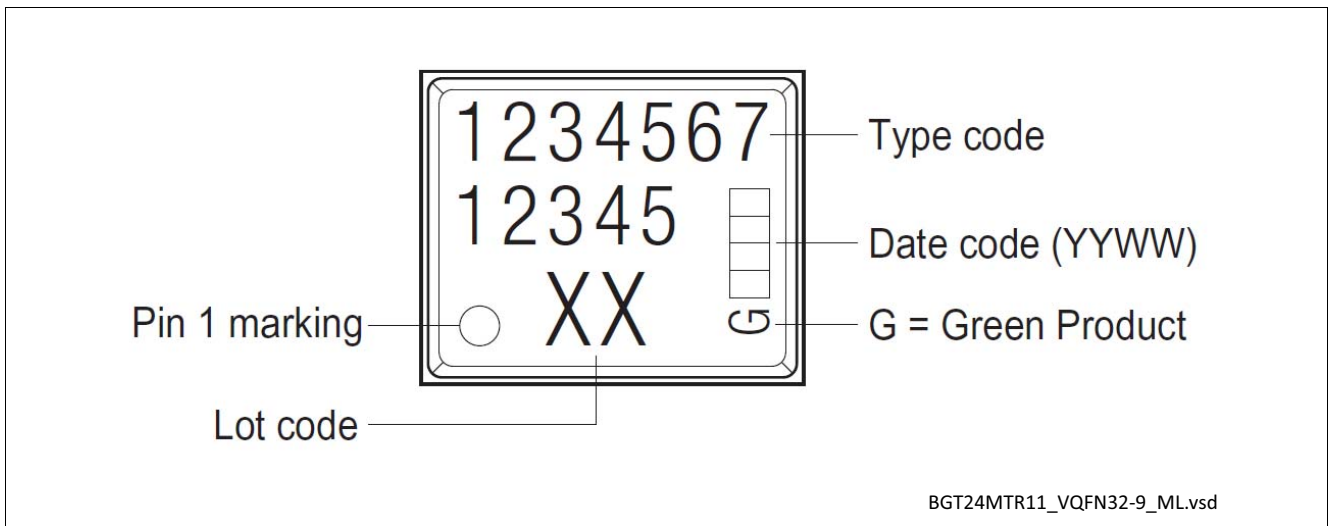
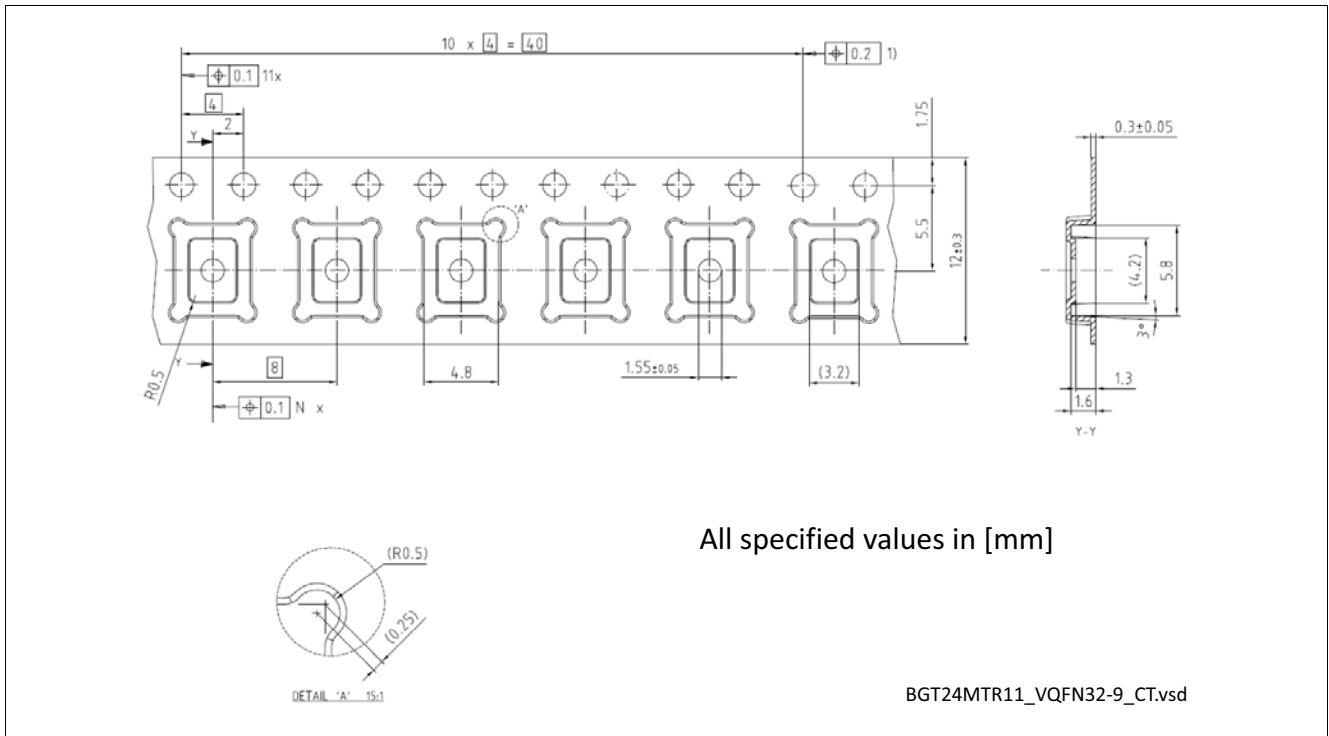


Figure 11 Marking Layout VQFN32-9



**Figure 12** Tape of VQFN32-9

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